CLAIMS

What is claimed is:

1. A transimpedance amplifier (TIA) circuit, comprising:

a first opamp having an input and an output;

a second opamp having an input that communicates with an output of said first opamp and an output;

a first feedback path that communicates with said input and said output of said first opamp and that includes a first resistance;

a second feedback path that communicates with said input and said output of said second opamp and that includes a second resistance; and

a third feedback path that communicates with said input of said first opamp and said output of said second opamp.

2. The TIA circuit of Claim 1 wherein said first and second resistances are variable resistances that have resistance values that decrease as frequency increases.

3. The TIA circuit of Claim 1 wherein said first feedback path includes a first capacitance in parallel with said first resistance and wherein said second feedback path includes a second capacitance in parallel with said second resistance.

4. The TIA circuit of Claim 3 wherein said first feedback path further includes a third resistance in series with said first resistance.

5. The TIA circuit of Claim 4 wherein said third resistance has a resistance value that is approximately two times a resistance value of said first resistance.

6. The TIA circuit of Claim 4 wherein said first and third resistances have substantially equal resistance values.

7. The TIA circuit of Claim 3 wherein said second feedback path further includes a fourth resistance in series with said second resistance.

8. The TIA circuit of Claim 7 wherein said fourth resistance has a resistance value that is approximately two times a resistance value of said second resistance.

9. The TIA circuit of Claim 7 wherein said second and fourth resistances have substantially equal resistance values.

10. The TIA circuit of Claim 7 wherein said first and second capacitances have substantially equal capacitance values.

11. The TIA circuit of Claim 1 further comprising a third opamp having an input that communicates with said output of said first opamp and an output that communicates with said input of said second opamp.

12. The TIA circuit of Claim 1 wherein said third feedback path includes a fifth resistance.

13. The TIA circuit of Claim 11 further comprising third, fourth and fifth capacitances that have one end that communicates with said inputs of said first, second and third opamps, respectively.

14. The TIA circuit of Claim 1 further comprising a sixth capacitance that communicates with said output of said second opamp.

15. A preamplifier comprising said TIA circuit of Claim 1.

16. A hard disk drive comprising said preamplifier of Claim 15.

17. A variable gain amplifier comprising said TIA circuit of Claim 1.

18. A read channel circuit comprising said variable gain amplifier of Claim 17.

19. A transimpedance amplifier (TIA) circuit, comprising:

first amplifying means for amplifying and having an input and an output;

second amplifying means for amplifying and having an input that communicates with said first amplifying means and an output;

first feedback means for providing feedback and that communicates with said input and said output of said first amplifying means and that includes first resistance means for providing a resistance;

second feedback means for providing feedback and that communicates with said input and said output of said second amplifying means and that includes a second resistance means; and

third feedback means for providing feedback and that communicates with said input of said first amplifying means and said output of said second amplifying means.

20. The TIA circuit of Claim 19 wherein said first and second resistance means provide variable resistances that decrease as frequency increases.

21. The TIA circuit of Claim 19 wherein said first feedback means includes first capacitance means for providing capacitance in parallel with said first resistance means and wherein said second feedback means includes second capacitance means for providing capacitance in parallel with said second resistance means.

22. The TIA circuit of Claim 21 wherein said first feedback means further includes third resistance means for providing resistance in series with said first resistance means.

23. The TIA circuit of Claim 22 wherein said third resistance means has a resistance value that is approximately two times a resistance value of said first resistance means.

24. The TIA circuit of Claim 22 wherein said first and third resistance means have substantially equal resistance values.

25. The TIA circuit of Claim 21 wherein said second feedback means further includes fourth resistance means for providing a resistance in series with said second resistance means.

26. The TIA circuit of Claim 25 wherein said fourth resistance means has a resistance value that is approximately two times a resistance value of said second resistance means.

27. The TIA circuit of Claim 25 wherein said second and fourth resistance means have substantially equal resistance values.

28. The TIA circuit of Claim 21 wherein said first and second capacitance means have substantially equal capacitance values.

29. The TIA circuit of Claim 19 further comprising third amplifying means for amplifying and having an input that communicates with said output of said first amplifying means and an output that communicates with said input of said second amplifying means.

30. The TIA circuit of Claim 19 wherein said third feedback means includes fifth resistance means for providing resistance.

31. The TIA circuit of Claim 29 further comprising third, fourth and fifth capacitance means for providing capacitance and that have one end that communicates with said inputs of said first, second and third amplifying means, respectively.

32. The TIA circuit of Claim 19 further comprising sixth capacitance means for providing capacitance and that communicates with said output of said second amplifying means.

33. A preamplifier comprising said TIA circuit of Claim 19.

34. A hard disk drive comprising said preamplifier of Claim 33.

35. A variable gain amplifier comprising said TIA circuit of Claim 19.

36. A read channel circuit comprising said variable gain amplifier of Claim 35.

37. A method for operating a transimpedance amplifier (TIA) circuit, comprising:

providing first and second amplifier stages, each having inputs and outputs;

feeding back an output of said first amplifier stage to said input of said first amplifier stage via a first resistance;

feeding back an output of said second amplifier stage to said input of said first amplifier stage via a second resistance; and

feeding back said output of said second amplifier stage to said first amplifier stage.

38. The method of Claim 37 further comprising lowering a first resistance value of said first resistance at high frequencies relative to said first resistance value low frequencies.

39. The method of Claim 37 further comprising lowering a second resistance value of said second resistance at high frequencies relative to said second resistance value low frequencies.

40. The method of Claim 37 further comprising providing a third amplifier stage between said first and second amplifier stages.

41. The method of Claim 37 further comprising implementing said first resistance using a third resistance in parallel with a first capacitance and a fourth resistance in series with said third resistance.

42. The method of Claim 37 further comprising implementing said second resistance using a fifth resistance in parallel with a second capacitance and a sixth resistance in series with said fifth resistance.

43. The method of Claim 41 further comprising setting said fourth resistance to a fourth resistance value that is approximately two times a third resistance value of said third resistance.

44. The method of Claim 42 further comprising setting said sixth resistance to a sixth resistance value that is approximately two times a fifth resistance value of said fifth resistance.

45. The method of Claim 41 further comprising setting said third and fourth resistances to substantially equal resistance values.

46. The method of Claim 42 further comprising setting said fifth and sixth resistances to substantially equal resistance values.